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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/717,386	11/18/2003	Prakash Narain	59165-298553	7467

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EXAMINER	
SIEK, VUTHE	
ART UNIT	**PAPER NUMBER**
2825	

DATE MAILED: 04/24/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/717,386	NARAIN ET AL.	
	Examiner	Art Unit	
	Vuthe Siek	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 November 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-7* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1 and 2* is/are rejected.

7)☒ Claim(s) *3-7* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *11/18/03;8/29/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This office action is in response to application 10/717,386 filed on 11/18/2003. Claims 1-7 remain pending in the application.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

3. Claim 1 is rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. The step of "automatically generating a plurality of design verification checks for use in connection with model checking, the plurality of design verification checks based upon application a set of one or more predetermined properties to the language-based representation of the hardware design" is not described in the specification. There is no description of such of verification checks for use in connection with model checking as originally filed.

4. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

5. Claim 1 is rejected under 35 U.S.C. 112, second paragraph, as being incomplete for omitting essential structural cooperative relationships of elements, such omission amounting to a gap between the necessary structural connections. See MPEP

§ 2172.01. The omitted structural cooperative relationships are: "receiving a language-based representation of a hardware design **and information regarding to the design intent**" and "the application of predetermined properties to an annotated hardware design representation and to **signal propagation among all the sentinel variables results in an exhaustive list of checks that confirm whether or not the predetermined properties hold true for the intended flow of logical signals**". Claim 1 has claim construction problem because the claim does not have information of that should be claimed. For example, "comprehensive verification checks are automatically generated based upon application of a set of predetermined properties to an annotated hardware design representation and the application of the predetermined properties to signal propagation among all the sentinel variables to confirm the intended flow of signals as defined by designer's intent". Lacking these essential components results omitted structural cooperative relationships of components that must be used for the verification.

6. Claim 1 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. The step of "by determining whether one or more of the plurality of design verification checks are violated by the hardware design" is not understood because normally the design verification checks are used to verify whether the hardware design is violated by the checks. In addition, "a set of one or more predetermined properties" lacks proper claim antecedent basis.

Double Patenting

7. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970);and, *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

8. Claims 1-2 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-13 of U.S. Patent No. 6,493,852 B1. Although the conflicting claims are not identical, they are not patentably distinct from each other because the patent claims refer to a method comprising inferring the existence of potential errors in the hardware design based upon the designer's expressed or implied intent regarding the intended flow of logical signals among the one or more variable by automatically generating a plurality of verification checks based upon designer/s expressed or implied intent, each check representing a condition that must be hold true in order for the hardware design to operate in accordance with the intended flow of the logical signals and determining if any of the checks can be violated during operation of circuitry represented by the hardware design. The patent claims are not teach model checking. However, the model checking is well known as admitted by applicants to verify properties of a circuit design. Therefore, it would have been obvious

to practitioners in the art to verify the circuit design using the generated checks as taught in the patent claims in connection with model checking in order to verify the properties of the circuit design in accordance with designer's intent and generated checks.

9. Claims 1-2 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-55 of U.S. Patent No. 6,529,523 B1. Although the conflicting claims are not identical, they are not patentably distinct from each other because the patent claims refer to a method comprising receiving information regarding an intended flow of logical signals in a hardware design, the intended flow including an indication of one or more variable in a language representation of the hardware design through which the logical signals pass and an indication of one more conditions under which each of the one or more conditions under which each of the one or more variables are to be associated with each of states and formulating a plurality of checks based upon a predetermined set of properties that must hold true in order for the hardware design to operate in accordance with the intended flow, conclusions regarding each of the checks being inferred based upon the states associated with the one or more variables during propagation of the logical signals. The patent claims are not teach model checking. However, the model checking is well known as admitted by applicants to verify properties of a circuit design. Therefore, it would have been obvious to practitioners in the art to verify the circuit design using the generated checks as taught in the patent claims in connection with model checking in

order to verify the properties of the circuit design in accordance with designer's intent and formulated checks.

Claim Rejections - 35 USC § 102

10. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

11. Claims 1-2 are rejected under 35 U.S.C. 102(e) as being anticipated by Ly et al. (6,175,946).

12. As to claim 1, Ly et al. teach a method for automatically generating checkers (design verification checks) for finding functional defects in a description of a circuit (a language-based representation of a hardware design (see abstract). The method comprising receiving a language-based representation of a hardware design (Fig. 1A, description of circuitry); automatically generating a plurality of design verification checks (automatically generating checkers) for use in connection with model checking (related checkers or simulation), the plurality of design verification checks based upon application of a set of one or more predetermined properties (known defective behavior) to the language-based representation of the hardware design; verifying the hardware design, as implemented according to the language-based representation, against

intended behavior, represented by the set of one or more predetermined properties, by determining whether one or more of the plurality of design verification checkers are violated by the hardware design (the checker monitors behavior of the instance, the signals flowing to and/or from the circuit elements for conformance with the known defective behavior); and reporting results of the verifying (the checker generates an error message) (at least see summary).

13. As to claim 2, Ly et al. teach a hardware description (for example Verilog or VHDL) (col. 6, lines 46-54).

Claim Rejections - 35 USC § 103

14. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

15. Claims 1-2 are rejected under 35 U.S.C. 103(a) as being unpatentable over Switzer et al., "Using Embedded Checkers to Solve Verification Challenges," (DesignCon2000), pages 1-20.

16. As to claims 1-2, Switzer et al. teach using embedded checkers to verify the intended flow of signals of an IC design (see whole document). The checkers are inserted as comments in the HDL generated initially from RTL source code and used to verify the properties of the intended flow of signals through the IC design. Switzer et al.

do not teach model checking. However, the model checking is well known in the art as admitted by applicants and used to verify properties of a circuit design. Therefore, it would have been obvious to practitioners in the art to verify the circuit design using the embedded checkers as taught by Switzer et al. in connection with model checking in order to verify the properties of the circuit design in accordance with designer's intent and embedded checkers.

Allowable Subject Matter

17. Claims 3-7 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims and if rewritten to overcome the rejection(s) under 35 U.S.C. 112, first and second paragraphs, set forth in this Office action. The prior art of record does the predetermined properties include a block enable property that relates to whether conditions enabling execution of a particular blocks of code in the RTL source will never be satisfied; an assignment execution property that relates to checking wither each logical value is assigned to a variable in the RTL source code through assignment operations appearing in the RTL source code; a conflicting assignment property that relates to checking whether it is possible for a write in the hardware design to be driven by multiple conflicting drivers; a constant value memory element property that relates to determining whether a memory element in the hardware design will always hold a constant value; and a constant value variable property that

relates to determining whether a variable in the RTL source code will always hold a constant value.

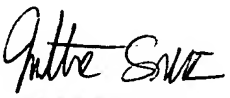
Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Vuthe Siek whose telephone number is (571) 272-1906.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jack Chiang can be reached on (571) 272-7483. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Vuthe Siek



VUTHE SIEK
PRIMARY EXAMINER